REMARKS

Applicant is including a proposed drawing correction in the same package with the present Amendment. In this proposed drawing correction, Applicant is amending Figs. 1A-1D to include the legend "Prior Art", as suggested by the Examiner.

Claims 8-11 have been rejected under 35 U.S.C. 102(b) as being anticipated by Manning et al. (U.S. Patent No. 5,909,617).

Claim 8 has been amended to recite "wherein the silicide strap comprises a refractory metal layer reacted with semiconductor material in the conductive element, the dielectric spacer and the semiconductor substrate." Support for this amendment is found in the specification as originally filed at paragraphs 23 and 24 of the specification as originally filed. No new matter is added.

In contrast, Manning et al. teaches that a polysilicon layer 80 is deposited over the gate 76, the adjacent sidewall spacer and the drain 78 (Manning et al., Col. 7, lines 5-12; Fig. 9.) Regions 94 of polysilicon layer 80 are subsequently doped. (Manning et al., Col. 7, lines 30-32; Fig. 11.) Metal layer 100, most preferably titanium, is deposited over polysilicon 94. (Manning et al., Col. 7, lines 53-55; Fig. 12.) The structure is then sintered, such that the titanium reacts with the adjacent polysilicon layer 94 to form a silicide 110. (Manning et al., Col. 7, lines 58-62; Fig. 13.) For example, a silicide strap 114 electrically connects the gate 76 and drain 78. (Manning et al., Col. 8, lines 11-12.) However, unreacted portions of the polysilicon layer remain after the sintering step. (See, Manning et al., Fig. 13; Col. 8, lines 5 and 8-10.)

Because Manning et al. teaches that the silicide strap 114 is formed by reacting metal layer 100 with a portion of the underlying polysilicon region 94, Manning et al. fails to teach "the silicide strap comprises a refractory metal layer reacted "with semiconductor material in the conductive element, the dielectric spacer and the semiconductor substrate" as recited by amended Claim 8. For this reason, amended Claim 8 is not anticipated by Manning et al.

Claims 9-11, which depend from Claim 8 are not anticipated by Manning et al. for at least the same reasons as Claim 8.

Claims 12-15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Manning et al. (U.S. Patent No. 5,909,617).

Claims 12-15, which depend from Claim 8, are allowable over Manning et al. for at least the same reasons as Claim 8.

Applicant has added new Claims 16-25.

Claim 16 is dependent on Claim 8 and recites "wherein the semiconductor material comprises amorphous silicon". Support for Claim 16 exists in the specification as originally filed at paragraph 20, lines 10-13.

Claim 17 is dependent on Claim 8 and recites "wherein upper surfaces of the conductive element, the sidewall spacer and the semiconductor substrate comprise an implanted semiconductor layer." Support for Claim 17 is found in the specification as originally filed at paragraph 20, lines 1-3.

Claim 18 is dependent on Claim 17 and recites "wherein the implanted semiconductor layer comprises silicon".

Support for Claim 18 is found in the specification as originally filed at paragraph 19, lines 1-2.

Independent Claim 19 recites "a continuous silicide strap directly contacting the conductive element, the dielectric spacer and the semiconductor substrate." Support for Claim 19 is found in the specification as originally filed at paragraph 20, lines 1-4, paragraph 25, lines 6-9 and Figs. 2H-2I.

Claim 20 is dependent on Claim 19 and recites "wherein the dielectric spacer is silicon-rich". Support for Claim 20 is found in the specification as originally filed at paragraph 15.

Independent Claim 21 recites "a semiconductor region dispersed in the upper surfaces of the conductive element, the dielectric spacer and the semiconductor substrate" and "a silicide strap formed in the semiconductor region". Support for Claim 20 is found in the specification as originally filed at paragraph 20, lines 1-4, paragraph 25, lines 6-9 and Figs. 2H-2I.

Claim 22 is dependent on Claim 21 and recites "wherein the dielectric spacer is silicon-rich". Support for Claim 22 is found in the specification as originally filed at paragraph 15.

Claim 23 is dependent on Claim 21 and recites "the semiconductor region comprises amorphous silicon". Support for Claim 22 is found in the specification as originally filed at paragraph 20, lines 10-13.

Claim 24 is dependent on Claim 21 and recites "the semiconductor region comprises an implanted semiconductor layer". Support for Claim 22 is found in the specification as originally filed at paragraphs 19-20.

Claim 25 is dependent on Claim 24 and recites "the implanted semiconductor layer comprises silicon". Support for Claim 25 is found in the specification as originally filed at paragraphs 19-20.

CONCLUSION

Claims 8-25 are pending in the present application. Reconsideration and allowance of these claims is respectfully requested. Attached is a document "VERSION WITH MARKINGS TO SHOW CHANGES MADE". If the Examiner has any questions or comments, he is invited to call the undersigned at (925) 895-3545.

Respectfully submitted,

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Jan. 25, 2002
Date

Carrie Reddick
Signature

VERSION WITH MARKINGS TO SHOW CHANGES MADE

TITLE

(Amended) "Conformal Surface Silicide Strap On Spacer [And Method Of Making Same].

CLAIMS

8. (Amended) A semiconductor structure comprising:

a semiconductor substrate;

a conductive element located over the semiconductor substrate;

a dielectric spacer located adjacent to a sidewall of the conductive element; and

a continuous silicide strap located over the conductive element, the dielectric spacer and the semiconductor substrate, wherein the silicide strap comprises a refractory metal layer reacted with semiconductor material in the conductive element, the dielectric spacer and the semiconductor substrate.